Position-Specified Formation of Epitaxial Si Grains on Thermally Oxidized Si(001) Surfaces via Isolated Nanodots

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We report position-specified fabrication of epitaxial Si grains on an amorphous thermal oxide layer on Si(001) substrates. This process takes advantage of unique features of surface-sensitive deposition chemistry and nanoscale oxidation phenomena. To make the grown grains epitaxial with respect to the Si substrate, growth was initiated from Si nanodots that had been isolated from the substrate by the oxidation of mushroom-shaped overgrown structures. The position of each grain is controlled by the use of a lithographically patterned mask layer. Mechanisms of the oxidation-induced nanodot isolation, which is a key step in this fabrication process, are discussed. The present technique is applicable to the integration of various single-crystal materials onto Si substrates.

Introduction

Single-crystal substrates are used to fabricate a variety of electronic and photonic devices. While the thickness of commercially available single-crystal wafers is typically hundreds of microns, many devices utilize only the surface portion of the substrates. Once the device fabrication is completed, the bulk part of the substrate has no function other than as a mechanical support or an electrical contact. For example, compound-semiconductor wafers serve only as a crystalline template to grow heteroepitaxial structures for lasers and high-speed transistors.[1] Another example is silicon-on-insulator (SOI) wafers, in which a thin layer of single-crystal Si is separated from the substrate by an insulating oxide layer. Separation of the device regions from the substrate bulk improves electrical performance, as was demonstrated for high-power or high-voltage devices and complementary metal−oxide−silicon (CMOS) transistors.[2] Such benefits and the recent availability of high-quality SOI wafers have been accelerating implementation of the SOI technology into commercial production.

The above-mentioned considerations and technological trends were the motivation for us to conceive a versatile technology for forming single-crystal grains of various materials on commonly available substrates such as crystalline Si. If grown grains are large enough to accommodate a unit device, they can serve as an alternative substrate to conventional bulk wafers. In this paper, we report the formation of homoepitaxial Si grains on thermally oxidized Si wafers. The process we propose takes advantage of the unique features of selective-area deposition chemistry and nanoscale oxidation phenomena.

Nine steps of the fabrication process of our target structure, i.e., epitaxial Si grains on a thermally oxidized Si substrate, are illustrated in Scheme 1. We begin the process by forming a thermal oxide layer on a Si(001) substrate that serves as a mask for selective epitaxial growth (step i). A positive resist layer of poly(methyl methacrylate) (PMMA) is applied, and the window patterns are defined by electron-beam (EB) exposure followed by development in 4-methyl-2-pentanon (step ii). The patterns are transferred to the oxide mask by wet etching in an HF solution (step iii). Removal of the resist layer completes a mask layer of thickness t_m with a window dimension of D_w (step iv). Then, selective-area epitaxial growth of Si is carried out to form an overgrowth structure (step v). Removal of the oxide mask by an HF etching leaves a mushroom-shaped Si structure of height H and lateral overgrowth dimension L_g (step vi). By thermally oxidizing this mushroom-shaped structure, a Si nanodot is isolated from the substrate, preserving its epitaxial relationship with respect to the substrate (step vii). After the dot is exposed by etching the oxide layer (step viii), the second selective-area epitaxial growth is carried out to complete the target structure (step ix).

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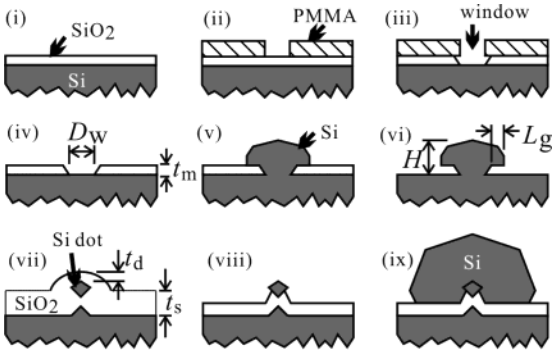
Scheme 1. Process Flow for Forming Epitaxial Si Grains on a Thermal Oxide Layer on Si[a]



[a] Epitaxial growth of a mushroom-shaped overgrown structure (steps i−vi), formation of an isolated Si nanodot by thermal oxidation (step vii), and epitaxial regrowth to form the final structure (steps viii and ix).

We use the (001) face of crystalline Si to demonstrate the process shown in Scheme 1; however, the same process is in principle applicable to other faces as well. Extension of the presented process to heteroepitaxial systems is straightforward, as discussed in the last part of this paper.

Experimental Section

Substrate Cleaning. Si(001) substrates (p-type; 1−10 Ω·cm) were cleaned for 10 min in a 1:0.25:5 mixture of 30 wt % aqueous H_2O_2, 29 wt % aqueous NH_3, and deionized water at 80 °C. After etching the chemical oxide in 1.0 wt % aqueous HF, followed by rinsing in deionized water, the wafer received another cleaning in a 1:1:5 mixture of 30 wt % aqueous H_2O_2, 36 wt % aqueous HCl, and deionized water at 80 °C for 10 min. The substrate was rinsed in deionized water and blown dry by filtered N_2 gas.

Thermal Oxidation in Steps i and vii. Thermal oxidation was carried out in O_2 gas (99.999 95% purity) at atmospheric pressure using a quartz-tube furnace. To form the mask layer in step i, oxidation was carried out for 10 min at 850 °C. For isolation of the Si nanodot in step vii, oxidation was continued for 3 h at 900 °C. The thickness of the formed oxide layers, t_m and t_s, as defined in Scheme 1, was 3.5 and 40 nm, respectively.[3]

EB Lithography. A PMMA resist layer was applied to the wafer surface by spin coating. Prior to PMMA application, the wafer surface was dehydrated using a hot plate kept at 175 °C. PMMA was dissolved in anisole. The viscosity of this solution was 50 cP. A 200-nm-thick layer of PMMA was obtained at a spin rate of 5000 rpm. PMMA-coated samples were baked at 175 °C for 40 min. Spot irradiation by EB, which was focused to approximately 20 nm in diameter, was carried out with typically 300-nm spacing to form a square array of irradiated spots. Beam energy and current were 30 keV and 30 pA, respectively. Each spot was irradiated for 60 μs, which translates into an estimated electron exposure of 0.6 mC/cm^2. For some experimental runs, line-and-space patterns were also formed. A line was drawn by repeating a spot irradiation for 8 μs followed by a 5-nm beam shift in the line direction. The average electron exposure for the line patterns was 0.3 mC/cm^2. These EB exposure levels were close to those typically used for PMMA.[4] Development was carried out by immersing the samples in a 1:1 mixture of 4-methyl-2-pentanone and 2-propanol for 80 s, followed by rinsing in 2-propanol. After oxide etching in step iii, the PMMA layer was removed by immersing the samples in acetone using an ultrasonic bath. To minimize redeposition of dissolved PMMA upon evaporation of acetone from the surface, immersion was repeated four times using virgin acetone solvent for each immersion. The sample surface received a final cleaning in a 1:1:5 mixture of 30 wt % aqueous H_2O_2, 36 wt % aqueous HCl, and deionized water at 80 °C for 10 min, followed by a rinse in deionized water.

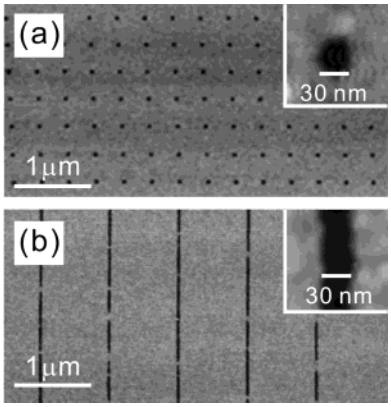


Figure 1. AFM images of the dot-array (a) and line-and-space (b) patterns defined on the SiO_2 mask layer (step iv of Scheme 1). Opened windows appear dark on these images. A magnified image of the window area is shown as an inset in each frame.

Oxide Etching in Steps iii, vi, and viii. Selective etching of SiO_2 to Si in steps iii, vi, and viii was carried out using an aqueous solution of HF. In step iii, windows were opened through the 3.5-nm-thick oxide mask layer by etching in a 1.0 wt % HF solution. Since this solution etched the thermal oxide at a rate of 0.08 nm/s, the etching time was set at 50 s. Oxide etching in step vi was carried out using an HF solution of a higher concentration, 5 wt %, and for a longer time, 200 s, since the etching depth for this step was L_g, as defined in Scheme 1 (typically 20 nm), instead of t_m. In step viii, the isolated nanodot was exposed by etching in a 1.0 wt % solution for 230 s.

Selective-Area Epitaxial Growth in Steps v and ix. Epitaxial growth of Si was carried out using a Si_2H_6 source gas in a cold-wall reactor in which the background pressure was in the 10^{-8} Pa range. Growth selectivity was achieved by employing the so-called ultrahigh vacuum (UHV) chemical vapor deposition (CVD) technique.[5,6] The Si_2H_6 pressure was set at 0.011 Pa. The sample temperature was kept at 590 °C by radiation heating from an SiC heater element. The growth time was 600 s. These conditions were common to steps v and ix. Prior to each epitaxial growth run, the wafer was etched in a 1.0 wt % HF solution for 5 s to ensure an oxide-free Si surface in the growth area. After the HF-etched sample was loaded into the CVD apparatus, it was first treated by $SiCl_4$ adsorption[7] and was subsequently subjected to Si epitaxial growth processing. The $SiCl_4$ treatment passivates the OH groups on the HF-etched oxide, which otherwise serve as nucleation centers in Si CVD.[8,9] Procedures and conditions of the $SiCl_4$ treatment are given in ref 7.

Results and Discussion

Dimensions of Growth Windows. The topography of the patterned mask layers (step iv of Scheme 1) was observed by tapping-mode atomic force microscopy (AFM). Images of the dot-array and line-and-space

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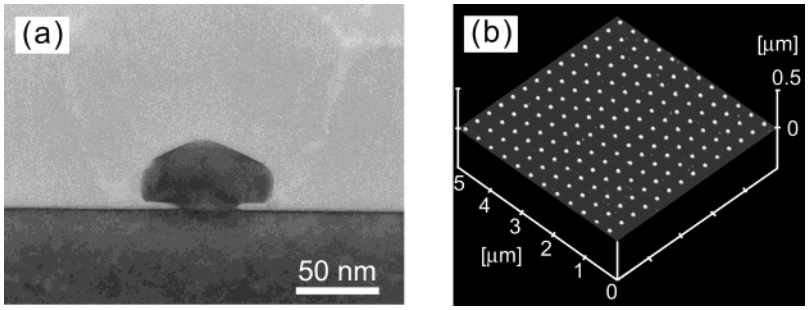

Figure 2. Mushroom-shaped structure of Si formed by selective-area epitaxial growth and the subsequent oxide mask removal (step vi in Scheme 1). (a) Cross-sectional TEM image. (b) AFM image of the mushroom-shaped structures arranged in an array pattern.

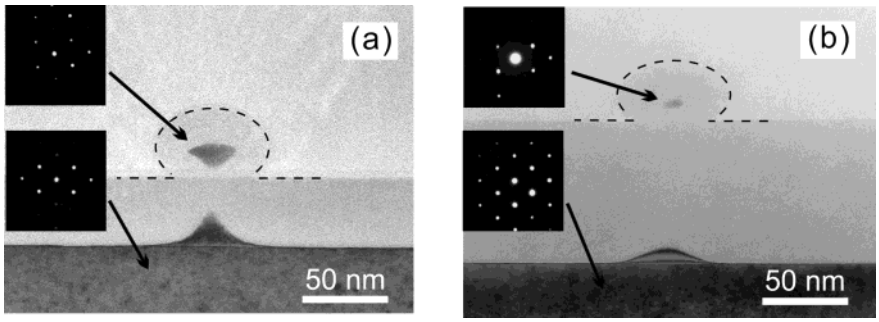

Figure 3. Isolated Si nanodots (step vii in Scheme 1) as observed by a cross-sectional TEM. Images a and b are for the samples oxidized at 900 °C for 3 h and at 950 °C for 4.5 h, respectively. Insets in each picture show TED patterns for the nanodot and substrate. Beam projection in the TEM/TED observation was along [110].

patterns are shown in parts a and b of Figure 1, respectively. Magnified images of the growth windows are shown in the inset in each frame. The dot diameter and line width both measure 30 nm. This size is comparable to those reported for windows defined by a similar technique.[10] The window size is determined by two factors: resolution of the EB exposure in step ii and setback of the window edge during the pattern transfer in step iii. The extent of the setback is comparable to the thickness of the oxide mask (3.5 nm in this study), because the Hf etching is isotropic. The window size in Figure 1 is therefore determined primarily by the lithography resolution (approximately 20 nm). Although the setback of the window edge could be minimized by the use of anisotropic plasma etching, we did not choose the plasma process, because it degrades the growth selectivity of the oxide mask.[11]

Selective Epitaxial Growth of Mushroom Structures. A TEM image of a cross section of an epitaxially grown structure in step vi is shown in Figure 2a. We find that lateral overgrowth on the mask surface forms a mushroom-like structure with ⟨113⟩ facets on its pileus part. The diameter of the neck part is 35 nm, which agrees with the window opening shown in Figure 2a. The appearance of the ⟨113⟩ facets is commonly observed for epitaxial growth of Si.[12,13] An AFM image of an array of mushroom structures is shown in Figure 2b. Si nucleation on the HF-etched oxide surface is suppressed, which verifies the effectiveness of the $SiCl_4$ pretreatment.

Isolation of Nanodots by Thermal Oxidation. The mushroom structures were thermally oxidized to form isolated nanodots as illustrated in step vii of Scheme 1. A TEM image of a sample oxidized at 900 °C for 3 h is shown in Figure 3a. The pileus of the mushroom structure is indeed isolated from the substrate to form a nanodot, while the neck is completely converted into oxide. The height and lateral size of the isolated dot measure 30 and 20 nm, respectively. Beneath the dot, a volcano-shaped Si structure remains as a result of the isolation process.

A cross section for another sample that was oxidized at 950 °C for 4.5 h is shown in Figure 3b. For this particular sample, the mask patterning was carried out by a proximal probe technique as reported in our previous publication.[14] The size and shape of the resultant epitaxial structures were essentially the same as those in Figure 2. Compared to Figure 3a, the height and lateral size of the dot is now reduced to 10 and 5 nm, respectively, due to the higher temperature and longer period of oxidation. Moreover, the dot is further separated from the substrate while the volcano-shaped structure is less steep. The thickness of the oxide layer on the Si substrate is 83 nm, which is consistent with the reported kinetics of thermal oxidation.[15]

There are two important observations regarding the results in Figure 3. First, the isolated dots preserve the crystallographic orientation of the Si substrate. Transmission electron diffraction (TED) patterns of the dot and substrate of each sample are shown as insets in

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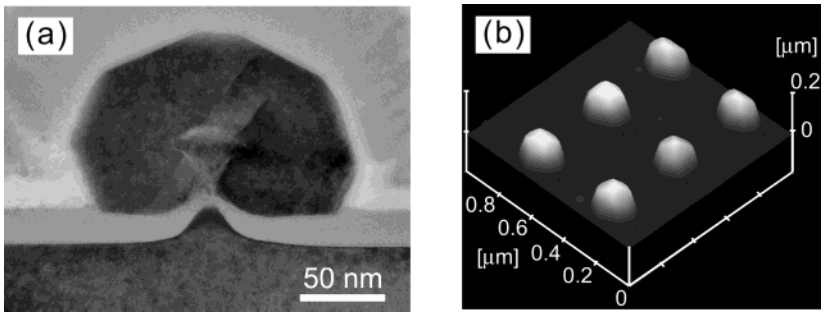

Figure 4. Epitaxial Si grains formed on the thermal oxide layer by regrowth of the isolated nanodots (step ix in Scheme 1). (a) Cross-sectional TEM image. (b) AFM image of an array of the grains.

Figure 3a,b. The projection direction was along [110]. These patterns indicate that the nanodots are epitaxial with respect to the substrate, even after they are separated from the substrate by an *amorphous* thermal oxide layer.

Second, we find that the oxide layer formed on top of the nanodots, t_d, is thinner than that on the substrate, t_s (see step vii in Scheme 1 for definitions of t_d and t_s). For oxidation of Si nanostructures, size- or pattern-dependent retardation is reported for particles,[16] wires,[17] and patterned structures on SOI substrates.[18,19] It has been suggested that local strain caused by volume expansion upon Si oxidation is responsible for this retardation effect.[20,21] The oxidation-induced strain accumulates to a greater extent in small or patterned structures than on a plain substrate due to geometrical reasons.

Because of the thickness difference between t_d and t_s, dot exposure in step viii can be accomplished simply by etching the sample just long enough to remove the oxide layer covering the dot but short enough to keep the wafer surface covered by the remaining oxide layer.

Selective Epitaxial Regrowth of Epitaxial Grains on Oxidized Surfaces. The target structure, as shown in step ix of Scheme 1, is formed by regrowth of the isolated nanodots. A cross-sectional TEM image of a grain formed on the oxide layer by the regrowth process is shown in Figure 4a. The initial nanodot was prepared by the same processes as had been used to form the nanodot shown in Figure 3a. As expected, the TED pattern (not shown in the figure) was identical to those in Figure 3a,b, verifying an epitaxial relationship between the grain and the substrate. An array of the facetted grains is formed with good growth selectivity, as shown in the AFM image in Figure 4b. Similarly to Figure 2a, the top surface of the grain consists of ⟨113⟩ faces.

In Figure 4a, ⟨111⟩ stacking fault defects are observed as dark lines. We ascribe the observed defect generation to residual oxide on the exposed nanodot surface. Stacking fault generation in Si homoepitaxy is often observed when the oxide removal on the Si substrate is insufficient.[22] Related to this issue, it was reported that defect generation in lateral overgrowth of Si is suppressed by keeping the growth temperature under 850 °C.[23] The growth temperature in the present study, however, is much lower than this temperature.

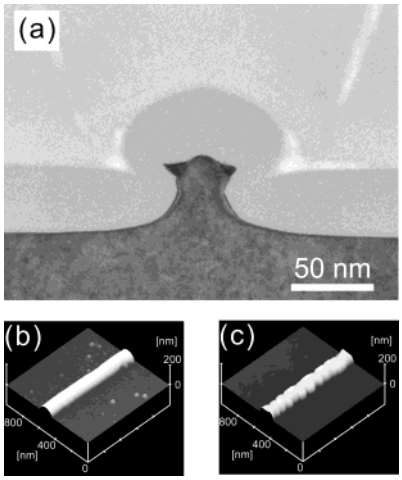

Figure 5. (a) Cross-sectional TEM image of an epitaxially grown line structure that was thermally oxidized at 900 °C for 3 h. (b) AFM image of the as-grown (i.e., no oxidation) line structure (step v in Scheme 1). (c) AFM image of the line structure that was thermally oxidized and then etched in HF. Edges of the line structure are rough as compared to those of part b.

The structure shown in Figure 4 can be regarded as locally formed SOI. For device applications of this structure, additional processing may be required to form a flat surface with a (001) orientation. A possible process for this purpose would be deposition of an insulating blanket layer of thickness larger than H followed by polishing.

Growth and Oxidation of Line-And-Space Structures. Now, we examine whether the present process is applicable to line-shaped structures. The mask pattern for preparation of the line structures is shown in Figure 1b. A cross-sectional TEM image for a line structure that underwent thermal oxidation at 900 °C for 3 h is shown in Figure 5a. The line-and-space structure was located next to the dot-array structure shown in Figure 3a, and the distance between them was only 0.1 mm. Thus, these two structures received

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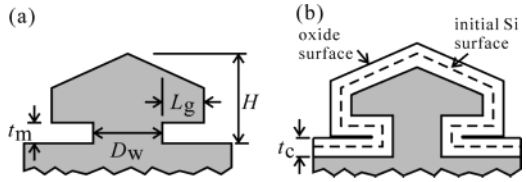

Figure 6. Schematic illustration of a cross section of the mushroom-shaped Si nanodot. (a) The as-grown structure. (b) An early stage of thermal oxidation when the oxide layer of thickness t_c just fills the gap between the overgrowth part and the substrate surface.

processing under identical conditions. In addition, the diameter of the dot-shaped mask opening and the width of the line-shaped opening were essentially equal, 30 nm, as was shown in Figure 1. Nonetheless, the isolation of the line structure was not successful, as shown in Figure 5a. This indicates that oxidation of the neck part of the line structure is significantly slower than that of the dot structures. We ascribe this difference to the fact that oxidation of the neck part proceeds one-dimensionally for the line structure (i.e., oxygen flux perpendicular to the line structure), while it proceeds two-dimensionally for the dot structure (i.e., oxygen flux from all lateral directions toward the dot structure).

In Figure 5a, two protrusions with dark contrast, which resemble dog ears, are formed on the line structure. The AFM image in Figure 5c reveals that many protrusions of a similar shape were formed on both sides of the line structure. This AFM image was taken after oxide removal (step viii), so the protrusions are clearly visible. For comparison, an AFM image for an as-grown Si line at step v is shown in Figure 5b. Both edges of the line structure are smooth in Figure 5b. The dark contrast of the protrusions in Figure 5a indicates that they have a different crystallographic orientation from that of the substrate and epitaxially grown line structure. Since it is unlikely that oxidation changes the crystallographic orientation of the Si crystal, we speculate that these structures were newly formed during the oxidation process by an accumulation of Si atoms supplied from other parts of the Si line structure. One possible source of Si supply is the emission of Si atoms from the Si−oxide interface, which was reported to occur to release the oxidation-induced stress.[24]

Mechanisms of Nanodot Isolation. Now, we discuss the mechanism of the nanodot isolation, which is the key step for fabricating the final structure of this study. We consider oxidation of a mushroom-like structure as illustrated in Figure 6a. As is widely known, oxidation of Si into SiO_2 is associated with a volume expansion by a factor of 2.3.[25] Consequently, the gap between the overgrowth part and the substrate surface (t_m in Figure 6a) becomes narrower as oxidation proceeds. The gap is filled when the oxide thickness reaches t_c, where $t_c(2.3 - 1)/2.3 = t_m/2$. This situation is depicted in Figure 6b. Further oxidation is possible only when the distance between the pileus part and the substrate is increased to accommodate the volume expansion. Thus, oxidation supposedly induces a tensile stress along the surface normal. This stress should accelerate thermal oxidation of the neck part, facilitating the nanodot isolation.[26]

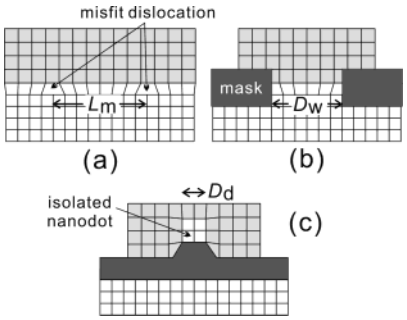

Figure 7. (a) Generation of misfit dislocations in lattice-mismatched heteroepitaxial systems. L_m is an average distance between two dislocation lines. (b) Possible suppression of the misfit dislocation by selective epitaxial overgrowth when D_w is smaller than L_m. (c) Proposed use of the isolated Si nanodot of size D_d as the nucleation site for dislocation-free heteroepitaxial growth.

Successful isolation of the nanodots depends on the shape of the initial mushroom structure, which is characterized by the four dimensions indicated in Figure 6a: H, L_g, D_w, and t_m. Since the neck part needs to be oxidized for isolation to be completed, it is apparent that smaller D_w is preferred as long as mechanical strength for supporting the entire mushroom structure is maintained. D_w, which was mainly determined by the resolution of EB lithography in this study, would increase in proportion to the setback upon isotropic etching in step iii. The extent of this setback is approximately equal to $2t_m$. Therefore, a smaller t_m is preferred to obtain a smaller D_w. In this study, t_m was maintained at 3.5 nm because an oxide thickness of less than 2 nm was difficult to control using our furnace.

L_g is another critical dimension for successful isolation of the nanodots. If L_g is too small, an oxide layer would be formed in a conformal manner over the mushroom structure and isolation would fail. On the other hand, if L_g is too large, neck oxidation would become slow because oxygen must diffuse a long way through the oxide-filled gap part of length $\sim L_g$ to reach the oxidation front.

Application to Heterostructure Fabrication. Extension of the present technique to heteroepitaxial systems is straightforward. Selective heteroepitaxial growth on Si was reported for a variety of materials including Ge,[27,28] SiGe,[29] SiC,[30] GaAs,[31] and GaN[32] among others. If we replace the second homoepitaxial growth in step ix with heteroepitaxial growth, single crystals of the material of interest can be formed in a similar form to that of Figure 4.

At the lattice-mismatched heterointerface, misfit dislocation is generated as illustrated in Figure 7a. Misfit dislocations often become nuclei for other types

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of defects, deteriorating the quality of the grown crystals. The average distance between the misfit dislocations, L_m, is inversely proportional to the lattice mismatch.[33] If D_w is smaller than L_m, the misfit dislocation generation can be suppressed, in principle, as illustrated in Figure 7b. A pioneering work on a dislocation-control technique by selective-area growth was reported by Nishinaga et al.[34] They proposed microchannel epitaxy (MCE), in which defect propagation is blocked by allowing the epitaxial growth only in (or from) microchannels. In a recent review on the MCE technique, the possibility of completely dislocation-free growth using nanoscale channels was discussed.[35] For nanoscale heteroepitaxial phenomena, Zubia et al. pointed out the importance of size-dependent strain energy and demonstrated a significant defect density reduction in the GaN/Si system.[36]

The success of such a defect control strategy critically depends on how small a window one can prepare for the selective-area growth. For instance, if the interplanar spacing of interest is a (004) spacing of Si (0.14 nm), a moderate mismatch of 1% gives an L_m as small as 14 nm. Defining such a small window is not an easy task, even if a state-of-the-art lithography facility is available. Selective-area growth onto isolated nanodots has a great advantage in this regard. The size of the isolated nanodot can be scaled down from the lithography feature size (30 nm in this study) to the sub-10 nm range by adjusting the extent of nanodot oxidation, as demonstrated in Figure 3b. Thus, the present process is suitable for forming nanoscale templates for dislocation-free heteroepitaxial growth.

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Conclusions

We demonstrated that epitaxial grains of Si can be formed at lithographically specified positions on thermally oxidized Si(001) wafers. To form this final structure, a mushroom-shaped overgrown structure was first formed by selective-area epitaxial growth using an oxide mask that had been patterned by EB lithography. By thermally oxidizing this mushroom structure, Si nanodots were separated from the substrate while their epitaxial relationship to the substrate was maintained. The final structure of single-crystal Si grains was formed by a second selective epitaxial growth. Application of the same processing to a line-shaped structure failed. Anomalous protrusions were formed at both edges of the oxidized line structure.

Although the structural integrity of the Si grains fabricated in this study is not yet as high as that of the state-of-the-art SOI wafers, future improvements will hopefully enable us to fabricate device-quality SOI structures at desired positions on plain Si wafers. By extending the presented scheme to heteroepitaxy, it will be possible for us to integrate electronic, photonic, and magnetic functions of various crystals onto Si substrates. A minimal amount of the materials of interest is needed to grow such heterostructures. Since many of the functional compound semiconductors are hazardous materials, the proposed heteroepitaxy approach is also attractive from the environmental point of view.

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